CLAIMS

1. A method of combining components to form an integrated device, comprising the following steps:

   - providing at least one first component on a first surface of a sacrificial substrate,
   - providing at least one second component on a first surface of a non-sacrificial substrate;
   - forming at least one support structure on at least one of said first surfaces of said sacrificial substrate, and said non-sacrificial substrate, respectively, such that said at least one support structure is extended outwardly from at least one of said first surfaces;
   - bonding said sacrificial substrate carrying said at least one first component, and said non-sacrificial substrate carrying said at least one second component, respectively, with an intermediate bonding material, so that said first and second surfaces will be facing one another with a distance essentially defined by a thickness of said support structure,
   - removing at least a part of said sacrificial substrate;
   - mechanically and/or electrically interconnecting said at least one first component and said at least one second component.

2. The method according to claim 1, further comprising the action of:
   - patterning said at least one first component after bonding said sacrificial substrate with said non-sacrificial substrate.

3. The method according to claim 1, further comprising the action of:
   - arranging a metal layer on a first surface of said at least one first component facing away from said non-sacrificial substrate after said bonding.

4. The method according to claim 1, further comprising the action of:
   - arranging a metal layer on a second surface of said at least one first component facing said non-sacrificial substrate prior to said bonding.

5. The method according claim comprising the action of:

- doping at least one first component made of semiconducting material and facing said non-sacrificial substrate prior to said bonding.

6. The method according to claim 3 and 4, wherein said metal layers on said first and second surfaces of said first component are of equivalent thickness.

7. The method according to claim 1, further comprising the action of:
   - providing at least one additional layer of stress compensating material on said first component.

8. The method according o claim 7, wherein said stress compensating material is at least one of the materials of: SiO2, SiN, metal.

9. The method according to claim 1, further comprising the action of:
   - performing said interconnection of said at least one second component with said at least one first component with the help of said at least one support structure.

10. The method according to claim 1, further comprising the action of:
    - securing said a least one first component to said non-sacrificial substrate with means other than said temporarily intermediate bonding material.

11. The method according to claim 10, further comprising the action of:
    - stripping away said intermediate bonding material.

12. The method according to claim 1, wherein said support structure is made of electrically non conducting material.

13. The method according to claim 1, wherein said support structure is made of electrically conducting material.

14. The method according to claim 12, further comprising the action of:
    - depositing an electrically conducting material on at least a portion of a surface of said support structure, prior to said bonding, for forming an

electrical connection between said at least one first component and said at least one second component .

15. The method according to claim 1, further comprising the action of:
performing said securing of said at least one first component to said non-sacrificial surface and said interconnection of said at least one first component with said at least one second component in a single action.

16. The method according to claim 1, wherein said first component and said non-sacrificial surface are secured to each other by one of the group of: evaporation, spin coating, sputtering, plating, riveting, soldering, gluing.

17. The method according to claim 1, wherein said intermediate bonding material is a low temperature adhesive, e.g. a polymer selected from poly-imide, benzocyclobutene (BCB), epoxy, photoresist.

18. The method according to claim 2, wherein said first component is a micro mirror.

19. The method according to claim 1, wherein said first component is made of single crystalline material.

20. The method according to claim 19, wherein said first component is made of single crystalline semiconducting material.

21. The method according to claim 1, wherein said second component is an integrated circuit.

22. The method according to claim 1, wherein said integrated device is a micro mirror Spatial Light Modulator (SLM) .

23 . The method according to claim 1, wherein said support structure is hollow with an open end.

24. The method according to claim 1, further comprising the action of:

- forming said support structure lithographically by patterning the intermediate bonding material prior to bonding.

25. The method according to claim 1, wherein the component 120 is at least partly prefabricated prior to bonding.

26. A Spatial Light Modulator having a plurality of micro mirror modulating elements, wherein said micromirrors are made of single crystalline material, and where support members electrically and/or mechanically interconnect said micromirrors to a substrate provided with at least one integrated circuit (made by but not limited to for example CMOS, bi-CMOS, bi-polar, and similar processes).

27. A Spatial Light Modulator according to claim 26, wherein said support members essentially define the distance between the micromirror and said substrate.

28. A Spatial Light Modulator having a plurality of micro mirror modulating elements, wherein said micro mirrors are made of high temperature annealed and/or high temperature deposited material, and where support members electrically and/or mechanically interconnect said micro mirrors to a substrate provided with at least one integrated circuit (made by but not limited to for example CMOS, bi-CMOS, bi-polar, and similar processes).

29. A Spatial Light Modulator having a plurality of micro mirror modulating elements, wherein said micro mirrors are made of single crystalline silicon, and where support members electrically and/or mechanically interconnect said micro mirrors to a substrate provided with at least one integrated circuit (made by but not limited to for example CMOS, bi-CMOS, bi-polar, and similar processes).

30. A Spatial Light Modulator having a plurality of micro mirror modulating elements, wherein said micro mirrors are made of single crystalline silicon germanium or single crystalline germanium or galium arsenide or indium phosphide or silicon carbide and where support members electrically and/or

mechanically interconnect said micro mirrors to a substrate provided with at least one integrated circuit (made by but not limited to for example CMOS, bi-CMOS, bi-polar, and similar processes).